Listing of Claims:

1. (Previously Presented) An integrated circuit comprising:

a two-dimensional pyramid filter architecture of an order 2N-1 to receive input signals, where N is a positive integer greater than two;

the two-dimensional pyramid filter architecture of order 2N-1 including;

one-dimensional pyramid filters of order 2N-1; and

a first summer circuit;

a second summer circuit;

said two dimensional pyramid filter architecture of order 2N-1, in operation, capable of producing, on respective clock cycles, at least the following:

pyramid filtered output signals corresponding to output signals produced by two one-dimensional pyramid filters of order 2N-1; and

a pyramid filtered output signal corresponding to an output signal produced summing signal sample matrices of order [2(N-1)-1] in the first summer circuit;

wherein the respective pyramid filtered output signals in said two dimensional pyramid filter architecture are summed by the second summer circuit on respective clock cycles of said two dimensional pyramid filter architecture.

2. (Currently Amended) The integrated circuit of claim 1, wherein N is three; and

wherein ~~said two dimensional pyramid filter architecture of order five, in operation, capable of producing, on respective clock cycles, the pyramid filtered output signals corresponding to the summation of four~~ the signal sample matrices comprise $P_{i-1,j-1}^{3x3}, P_{i-1,j+1}^{3x3}, P_{i+1,j-1}^{3x3}, P_{i+1,j+1}^{3x3}$ ~~and the output signals produced by a plurality of one-dimensional pyramid filters~~.

3. (Currently Amended) The integrated circuit of claim [[2]] 1, wherein said one-dimensional pyramid filters comprise a sequence of scalable cascaded multiplierless operational units, each of said operational units capable of producing a different order pyramid filtered output signal sample stream.

4. (Currently Amended) The integrated circuit of claim [[2]] 1, wherein said one-dimensional pyramid filters comprise other than one-dimensional multiplierless pyramid filters.

5. (Currently Amended) The integrated circuit of claim [[2]] 1, wherein the pyramid filtered output signals produced by a plurality of one-dimensional pyramid filters ~~being~~ are produced by eight one-dimensional pyramid filters of order three.

6. (Original) The integrated circuit of claim 5, wherein, of the eight one-dimensional pyramid filters of order three, four are applied row-wise and four are applied column-wise.

7. (Cancelled)

8. (Cancelled)

9. (Cancelled)

10. (Cancelled)

11. (Cancelled)

12. (Previously Presented) A method of filtering an image using a two-dimensional pyramid filter architecture of order 2N-1, where N is a positive integer greater than two, the two-dimensional pyramid filter architecture of order 2N-1 including one-dimensional pyramid filters of order 2N-1, said method comprising:

summing, on respective clock cycles of said two dimensional pyramid filter architecture, the following:

pyramid filtered output signals corresponding to output signals produced by two one-dimensional pyramid filters of order 2N-1; and

a pyramid filtered output signal corresponding to the summation of signal sample matrices of order [2(N-1)-1].

13. (Cancelled)

14. (Currently Amended) The method of claim 12, wherein N is three; and

wherein the ~~pyramid filtered output signals corresponding to the summation of four~~ signal sample matrices comprise $P_{i-1,j-1}^{3x3}, P_{i-1,j+1}^{3x3}, P_{i+1,j-1}^{3x3}, P_{i+1,j+1}^{3x3}$ ~~and pyramid filtered output signals produced by a plurality of one-dimensional pyramid filters~~.

15. (Currently Amended) The method of claim [[14]] 12, wherein said one-dimensional pyramid filters comprise a sequence of scalable cascaded multiplierless operational units, each of said operational units capable of producing a different order pyramid filtered output signal sample stream.

16. (Previously Presented) An article comprising: a storage medium, said storage medium having stored thereon instructions, that, when executed result in filtering an image using a two-dimensional pyramid filter architecture of order 2N-1, the two-dimensional pyramid filter architecture of order 2N-1 including one-dimensional pyramid filters of order 2N-1; where N is a positive integer greater than two, by:

summing, on respective clock cycles of said two dimensional pyramid filter architecture, the following:

pyramid filtered output signals corresponding to output signals produced by two one-dimensional pyramid filters of order 2N-1; and

a pyramid filtered output signal corresponding to the summation of signal sample matrices of order [2(N-1)-1].

17. (Cancelled)

18. (Currently Amended) The article of claim 16, wherein N is three; and

wherein the ~~pyramid filtered output signals corresponding to the summation of four~~ signal sample matrices comprise $P_{i-1,j-1}^{3x3}, P_{i-1,j+1}^{3x3}, P_{i+1,j-1}^{3x3}, P_{i+1,j+1}^{3x3}$ ~~and pyramid filtered output signals produced by a plurality of one-dimensional pyramid filters~~.

19. (Currently Amended) The article of claim [[18]] 16, wherein said one-dimensional pyramid filters comprise a sequence of scalable cascaded multiplierless operational units, each of said operational units capable of producing a different order pyramid filtered output signal sample stream.

20. (Previously Presented) An image processing system comprising:

an image processing unit to filter scanned color images; and

a summer circuit;

said image processing unit including at least one two-dimensional pyramid filter architecture;

said at least one two-dimensional pyramid filter architecture comprising:

a two-dimensional pyramid filter architecture of an order 2N-1, where N is a positive integer greater than two; the two-dimensional pyramid filter architecture of order 2N-1 including one-dimensional pyramid filters of order 2N-1;

said two dimensional pyramid filter architecture of order 2N-1, in operation, capable of producing, on respective clock cycles, at least the following:

pyramid filtered output signals corresponding to output signals produced by two one-dimensional pyramid filters of order 2N-1; and

a pyramid filtered output signal corresponding to the summation of signal sample matrices of order [2(N-1)-1];

wherein the respective pyramid filtered output signals in said two dimensional pyramid filter architecture are summed by the summer circuit on respective clock cycles of said two dimensional pyramid filter architecture.

21. (Cancelled)

22. (Currently Amended) The system of claim 20, wherein N is three; and

wherein the ~~pyramid filtered output signals corresponding to the summation of four~~ signal sample matrices comprise $P^{3x3}_{i-1,j-1}, P^{3x3}_{i-1,j+1}, P^{3x3}_{i+1,j-1}, P^{3x3}_{i+1,j+1}$ ~~and pyramid filtered output signals produced by a plurality of one-dimensional pyramid filters~~.

23. (Currently Amended) The system of claim [[22]] 20, wherein said one-dimensional pyramid filters comprise a sequence of scalable cascaded multiplierless operational units, each of said operational units capable of producing a different order pyramid filtered output signal sample stream.